

Attorney Docket No. 042390.P5120D

**REMARKS**

Both the title and the abstract have been objected to for being non-descriptive. The title and the abstract have both been amended accordingly. Withdrawal of the objections is respectfully requested.

Claims 19, 21, 23 and 26 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent no. 5,635,847 ("Seidel") in view of U.S. patent no. 5,483,421 ("Gedney") and further in view of U.S patent no. 5,680,936 ("Beers) and U.S. patent no. 5,983,490 ("Sakemi"). Applicants respectfully traverse these rejections because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

Independent claim 19 recites testing the cache memory devices on the interposer (emphasis provided), with a pass or fail by the cache memory devices determining whether the interposer and a microprocessor are coupled to a substrate. Contrary to the second paragraph of page 3 of the Office Action, Seidel does not disclose or suggest testing cache memory devices or any other type of active device. Seidel only discloses testing the solder connections (column 1 lines 27-31, 63-66). Siedel's only action with semiconductors is to burn them in (column 1 lines 63-66). By definition, the purpose of a burn-in is to age a device by applying power to it for a predefined time. No testing of functionality is required or implied, nor is any pass/fail operation implied by a simple burn-in.

None of the remaining references, either singly or in combination, disclose or suggest all the elements of claim 19.

Attorney Docket No. 042390.P5120D

Claims 21 and 26 depend from claim 19 and therefore contain the same limitations not disclosed or suggested by the cited references.

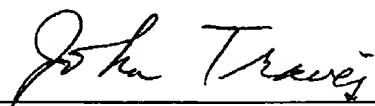
### CONCLUSION

For the foregoing reasons, Applicants submit that claims 19, 21 and 26 are now in condition for allowance, and indication of allowance by the Examiner is respectfully requested. Applicants further submit that claims 22, 24 and 25 should now be considered and found allowable in view of the allowance of claims 19, 21 and 26. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible. No fee is believed due in connection with this amendment. In this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

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**APPENDIX A****MARKED-UP COPY OF TITLE****[MULTI-CHIP LAND GRIP ARRAY CARRIER]****TESTING A MULTI-CHIP INTERPOSER****MARKED-UP COPY OF ABSTRACT****ABSTRACT**

[A land grid array (LGA) carrier includes an interposer having a first surface and a second surface opposite the first surface, with a plurality of locations on the first surface adapted to receive a plurality of semiconductor dice and passive components. The second surface has a plurality of conductive pads coupled thereto.]

An interposer with cache memory devices, a passive element, and conductive pads has solder balls attached to selected ones of the conductive pads. The cache memory devices are then tested, and the interposer is coupled to a substrate with the solder balls for further assembly only if the test is passed.

**MARKED-UP COPY OF AMENDED CLAIMS**

19. (Amended eight times) A method of assembling a multi-chip device comprising:  
[providing an interposer having a first surface and a second surface;]  
populating [the] a second surface of an interposer having a first surface and the  
second surface with a plurality of conductive pads;  
coupling solder balls to selected ones of the plurality of conductive pads;  
not coupling the solder balls to non-selected ones of the plurality of conductive  
pads;  
coupling a plurality of cache memory devices and at least one passive  
device to the first surface to form a multi-chip subassembly, wherein the at  
least one passive device is selected from a group consisting of resistors,  
capacitors, and inductors;  
testing said plurality of cache memory devices on said interposer;  
coupling said interposer to a substrate with the solder balls and coupling a  
microprocessor to the substrate after said testing if said plurality of cache memory devices  
pass said testing; and  
not coupling said interposer to the substrate and not coupling a microprocessor device  
to the substrate if said plurality of cache memory devices does not pass said testing.